What is claimed is:

1. A serial digital signal transmission system comprising a residual time stamp (RTS) generator circuit for separating high definition television (HDTV) serial digital signals to be transmitted into parallel data and time information residual time stamps (RTSs) and transmitting them as separated, and an RTS receiver circuit for receiving said parallel data and said time information RTSs that have been transmitted and obtaining said HDTV serial digital signals as they were originally, wherein:

said RTS generator circuit has:

first frequency dividing means for dividing a network clock into a prescribed first frequency,

a serial-to-parallel converter for subjecting said HDTV serial digital signals to be transmitted to serial-to-parallel conversion, transmitting data of the resultant parallel signals and supplying a clock divided into a second frequency,

a first counter for dividing said frequency-divided clock supplied from said serial-to-parallel converter into a 1/N frequency, and

a latch circuit for latching at the output timing of said first counter the clock resulting from the frequency division by said first frequency dividing means to supply said time information RTSs, and

said RTS receiver circuit comprises:

second frequency dividing means for dividing the frequency of said network clock into said prescribed first frequency,

gate pulse generating means for generating a gate pulse

on the basis of said network clock,

memory means for temporarily storing said RTSs which have been transmitted,

a comparator for comparing the clock resulting from frequency division by said second frequency dividing means and said RTSs read out of said memory means,

a gate circuit for gating the output signal of said comparator on the basis of said gate pulse from said gate pulse generating means,

frequency multiplying means for regenerating the clock of said second frequency by multiplying the frequency of the output signal of said gate circuit to said N-multiplied frequency, and

a parallel-to-serial converter for receiving as its inputs regenerated clock of said second frequency supplied from said frequency multiplying means and data of said parallel signals that have been transmitted, and subjecting these to parallel-to-serial conversion to obtain said HDTV serial digital signals, 8, 15 or 16 being selected as the value of said N.

2. The serial digital signal transmission system, as claimed in Claim 1, wherein said first frequency dividing means comprises a first frequency dividing circuit for dividing said network clock into a frequency of 1/32 and a first p-bit counter for counting clocks supplied from said first frequency dividing circuit and obtaining a signal of said prescribed first frequency, said second frequency dividing means comprises a second frequency dividing circuit for dividing said network clock into a frequency

of 1/32 and a second p-bit counter for counting clocks supplied from said second frequency dividing circuit and obtaining a signal of said prescribed first frequency, said gate pulse generating means is an M_q-$2^{(p-1)}$ counter (where M_q is the largest integer that does not surpass the average count M of the clock resulting from frequency division by 32 of the network clock in N periods of the serial clock of HDTV serial digital signals) for counting the clock supplied from said second frequency dividing circuit and supplying said gate pulse, and said frequency multiplying means is a PLL circuit for multiplying the frequency of the output signal of said gate circuit to said N-multiplied frequency.

3. The serial digital signal transmission system, as claimed in Claim 2, wherein said memory means is a FIFO storage whose read timing is determined by the output signal of said gate circuit and said M_q-$2^{(p-1)}$ counter is reset by the output signal of said gate circuit.

4. A serial digital signal transmission apparatus comprising a serial-to-parallel converter for separating high definition television (HDTV) serial digital signals to be transmitted into a parallel data and a first clock, a residual time stamp (RTS) generator circuit for generating time information RTSs on the basis of said first clock and a network clock, an ATM cell processing unit for assembling said RTSs and parallel data into asynchronous transfer mode (ATM) cells of a prescribed structure and transmitting the assembled cells and

separating received ATM cells of said prescribed structure into said RTSs and parallel data, an RTS receiver circuit for regenerating said first clock as they originally were on the basis of said separated time information RTSs and network clock, and a parallel-to-serial converter for obtaining said HDTV serial digital signals from said separated parallel data and said first clock from said RTS receiver circuit, wherein:

said RTS generator circuit has:

first frequency dividing means for dividing said network clock into a second clock of a prescribed frequency,

a first counter for dividing said first clock into a 1/N frequency, and

a latch circuit for latching at the output timing of said first counter the second clock resulting from the frequency division by said first frequency dividing means to supply said time information RTSs,

said RTS receiver circuit comprises:

second frequency dividing means for dividing the frequency of said network clock into said prescribed frequency,

gate pulse generating means for generating a gate pulse on the basis of said network clock,

memory means for temporarily storing said RTSs which have been transmitted,

a comparator for comparing the clock resulting from frequency division by said second frequency dividing means and said RTSs read out of said memory means,

a gate circuit for gating the output signal of said comparator on the basis of said gate pulse from said gate pulse

generating means, and

frequency multiplying means for regenerating said first clock frequency by multiplying the frequency of the output signal of said gate circuit to said N-multiplied frequency, wherein:

said ATM cell processing unit, besides selecting 8 as the value of said N, multiplexes 180 bytes of said HDTV serial digital signals on four of said ATM cells to generate ATM cells on whose remainder of payload are multiplexed nine of said time information RTSs corresponding to the 180 bytes of HDTV serial digital signals.

5. A serial digital signal transmission apparatus comprising a serial-to-parallel converter for separating high definition television (HDTV) serial digital signals to be transmitted into a parallel data and a first clock, a residual time stamp (RTS) generator circuit for generating time information RTSs on the basis of said first clock and a network clock, an ATM cell processing unit for assembling said RTSs and parallel data into asynchronous transfer mode (ATM) cells of a prescribed structure and transmitting the assembled cells and separating received ATM cells of said prescribed structure into said RTSs and parallel data, an RTS receiver circuit for regenerating said first clock as they originally were on the basis of said separated time information RTSs and network clock, and a parallel-to-serial converter for obtaining said HDTV serial digital signals from said separated parallel data and said first clock from said RTS receiver circuit, wherein:

said RTS generator circuit has:

first frequency dividing means for dividing said network clock into a second clock of a prescribed frequency,

a first counter for dividing said first clock into a 1/N frequency, and

a latch circuit for latching at the output timing of said first counter the second clock resulting from the frequency division by said first frequency dividing means to supply said time information RTSs,

said RTS receiver circuit comprises:

second frequency dividing means for dividing the frequency of said network clock into said prescribed frequency,

gate pulse generating means for generating a gate pulse on the basis of said network clock,

memory means for temporarily storing said RTSs which have been transmitted,

a comparator for comparing the clock resulting from frequency division by said second frequency dividing means and said RTSs read out of said memory means,

a gate circuit for gating the output signal of said comparator on the basis of said gate pulse from said gate pulse generating means, and

frequency multiplying means for regenerating said first clock frequency by multiplying the frequency of the output signal of said gate circuit to said N-multiplied frequency, wherein:

said ATM cell processing unit, besides selecting 8 as the value of said N, multiplexes 5500 bytes of said HDTV serial digital signals on 123 of said ATM cells to generate ATM cells on whose remainder of payload are multiplexed 275 of said time information

RTSs corresponding to the 5500 bytes of HDTV serial digital signals.

6. A serial digital signal transmission apparatus comprising a serial-to-parallel converter for separating high definition television (HDTV) serial digital signals to be transmitted into a parallel data and a first clock, a residual time stamp value (RTS) generator circuit for generating time information RTSs on the basis of said first clock and a network clock, an ATM cell processing unit for assembling said RTSs and parallel data into asynchronous transfer mode (ATM) cells of a prescribed structure and transmitting the assembled cells and separating received ATM cells of said prescribed structure into said RTSs and parallel data, an RTS receiver circuit for regenerating said first clock as they originally were on the basis of said separated time information RTSs and network clock, and a parallel-to-serial converter for obtaining said HDTV serial digital signals from said separated parallel data and said first clock from said RTS receiver circuit, wherein:

said RTS generator circuit has:

first frequency dividing means for dividing said network clock into a second clock of a prescribed first frequency,

a first counter for dividing said first clock into a 1/N frequency, and

a latch circuit for latching at the output timing of said first counter the second clock resulting from the frequency division by said first frequency dividing means to supply said time information RTSs,

said RTS receiver circuit comprises:

second frequency dividing means for dividing the frequency of said network clock into said prescribed frequency,

gate pulse generating means for generating a gate pulse on the basis of said network clock,

memory means for temporarily storing said RTSs which have been transmitted,

a comparator for comparing the clock resulting from frequency division by said second frequency dividing means and said RTSs read out of said memory means,

a gate circuit for gating the output signal of said comparator on the basis of said gate pulse from said gate pulse generating means, and

frequency multiplying means for regenerating said first clock frequency by multiplying the frequency of the output signal of said gate circuit to said N-multiplied frequency, wherein:

said ATM cell processing unit, besides selecting 15 as the value of said N, multiplexes 375 bytes of said HDTV serial digital signals on eight of said ATM cells to generate ATM cells on whose remainder of payload and RTS area of Segmentation and Reassembly Protocol Data Unit (SAR-PDU) header are multiplexed 10 of said time information RTSs corresponding to the 375 bytes of HDTV serial digital signals.

7. A serial digital signal transmission apparatus comprising a residual time stamp (RTS) generator circuit for separating high definition television (HDTV) serial digital signals to be transmitted into parallel data and time information

residual time stamps (RTSs) and for transmitting said parallel data and said them as separated, and an RTS receiver circuit for receiving said parallel data and said time information RTSs, wherein said RTS generator circuit has:

first frequency dividing means for dividing a network clock into a prescribed first frequency,

a serial-to-parallel converter for subjecting said HDTV serial digital signals to be transmitted to serial-to-parallel conversion, transmitting data of the resultant parallel signals and supplying a clock divided into a second frequency,

a first counter for dividing said frequency-divided clock supplied from said serial-to-parallel converter into a 1/N frequency, and

a latch circuit for latching at the output timing of said first counter the clock resulting from the frequency division by said first frequency dividing means to supply said time information RTSs